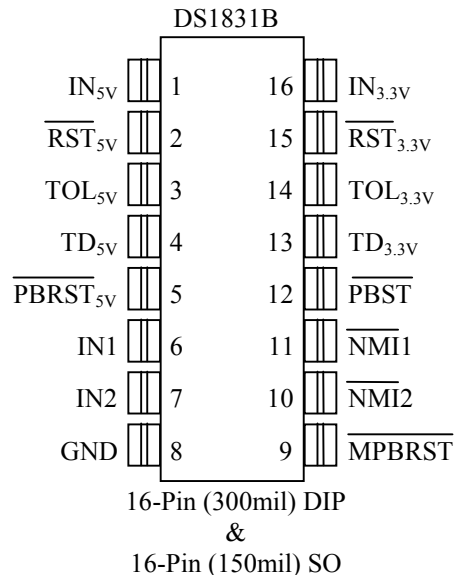
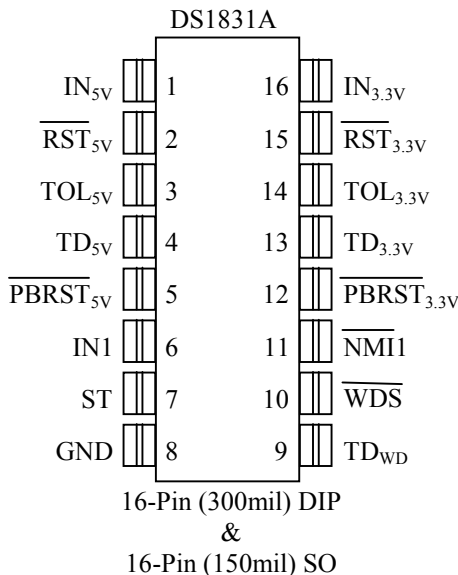
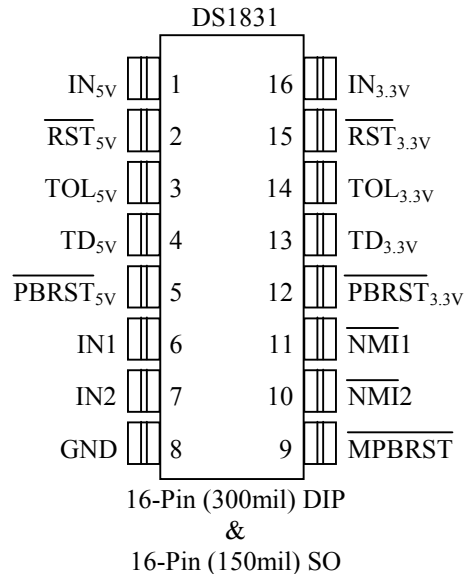


FEATURES

- 5V power-on reset
- 3.3V power-on reset
- Two referenced comparators with separate outputs for monitoring additional supplies
- Internal power is drawn from higher of either the IN_{5V} input or the IN_{3.3V} input
- Excellent for systems designed to operate with multiple power supplies
- Asserts resets during power transients
- Pushbutton reset input for system override
- Maintains reset for user configurable times of 10ms, 100ms, or 1s
- Watchdog timer for software monitoring (DS1831A)
- Precision temperature-compensated voltage reference and voltage sensor
- 16 pin DIP and 16 pin 150mil SO available
- Operating Temperature of -40°C to +85°C

PIN ASSIGNMENT



DESCRIPTION

The DS1831 multisupply monitor and reset monitors up to four system voltages: 5V supply, 3.3V (or 3V) supply, and two additional user configurable voltage monitors. DS1831 power for internal operation comes from the higher voltage level of the 3.3V input or the 5V input. One of these inputs must be greater than 1V for device operation. Pushbutton (manual reset) functionality is provided for the 5V reset, the

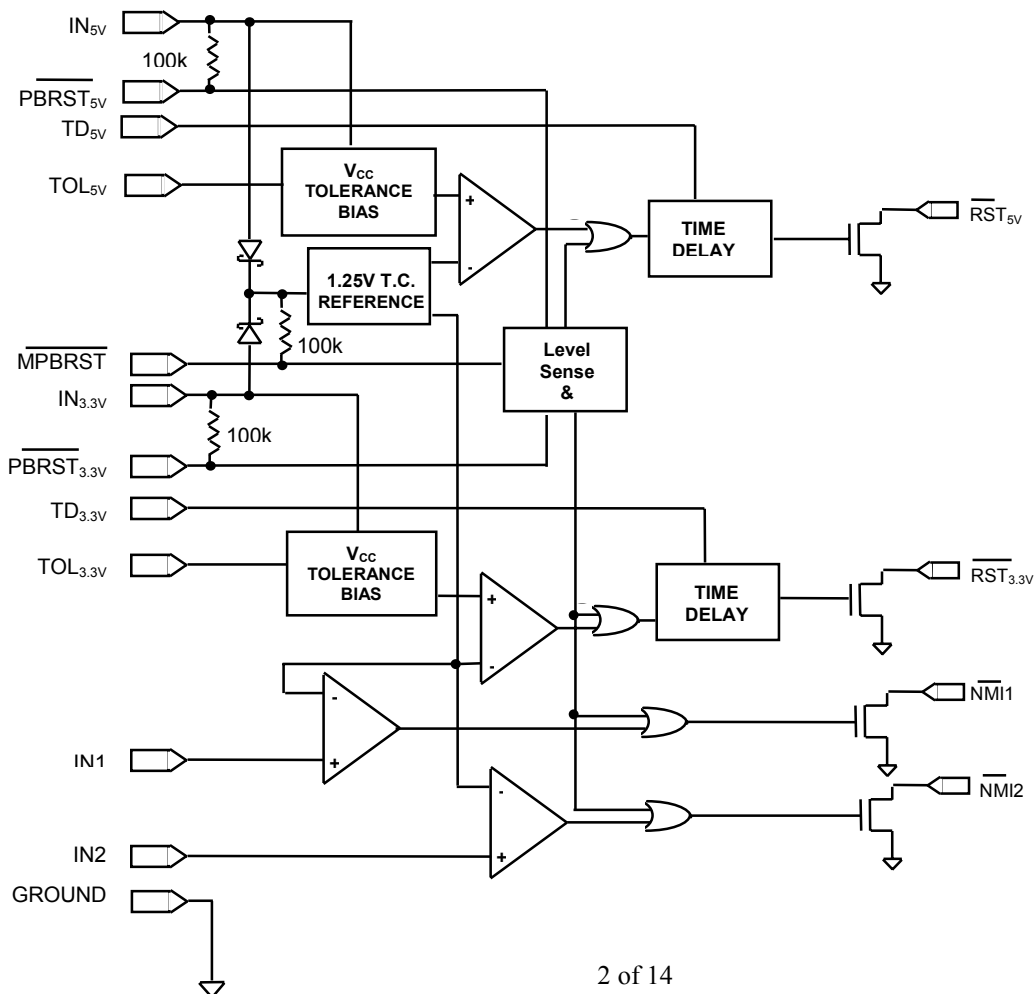
3.3V reset or for all reset outputs by the master pushbutton. The DS1831A replaces one reference comparator and the master pushbutton with watchdog and the DS1831B replaces the 3.3V $\overline{\text{PBRST}}$ with a last reset status output.

TOL and TD inputs allow user configuration of the DS1831 for multiple applications. The TOL inputs configure the tolerance for the specified output and the TD inputs configure the reset time delays.

PIN DESCRIPTION

$\text{IN}_{5\text{V}}$	5V Power Supply Input	MPBRST	Master Pushbutton (DS1831)
$\overline{\text{RST}}_{5\text{V}}$	5V Reset Open Drain Output	TD_{WD}	Watchdog Time Delay Select (DS1831A)
$\text{TOL}_{5\text{V}}$	Selects 5V Input Tolerance	$\overline{\text{NMI}}_2$	Non-maskable Interrupt 2 (DS1831)
$\text{TD}_{5\text{V}}$	Selects 5V Reset Time Delay	$\overline{\text{WDS}}$	Watchdog Status Output (DS1831A)
$\overline{\text{PBRST}}_{5\text{V}}$	5V Reset Pushbutton	$\overline{\text{NMI}}_1$	Non-maskable Interrupt 1
IN_1	Sense Input 1	$\overline{\text{PBRST}}_{3.3\text{V}}$	3.3V Reset Pushbutton
IN_2	Sense Input 2 (DS1831)	$\overline{\text{PBST}}$	Pushbutton Status Output (DS1831B)
ST	Watchdog Strobe Inputs (DS1831A)	$\text{TD}_{3.3\text{V}}$	Select 3.3V Reset Time Delay
GND	Ground	$\text{TOL}_{3.3\text{V}}$	Selects 3.3V Input Tolerance
		$\overline{\text{RST}}_{3.3\text{V}}$	3.3V Reset Open Drain Output
		$\text{IN}_{3.3\text{V}}$	3.3V Power Supply Input

DS1831 BLOCK DIAGRAM Figure 1



OPERATION—POWER MONITOR

The DS1831 provides the functions of detecting out-of-tolerance conditions on a 3.3V (or 3V) and 5V power supply and warning a processor-based system of impending power failure. When an input is detected as out-of-tolerance on either voltage input the $\overline{\text{RST}}$ for that supply will be forced active low. When that input returns to a valid state the associated $\overline{\text{RST}}$ will remain active for the time delay selected with the associated TD input and then return to an inactive state until the next input out-of-tolerance condition.

On power-up both resets are kept active for the selected reset time after the associated power supply input has reached the selected tolerance. This allows the power supply and system power to stabilize before $\overline{\text{RST}}$ is released.

All internal operating current for the DS1831 will be supplied by either the $\text{IN}_{3.3\text{V}}$ or $\text{IN}_{5\text{V}}$ input which ever has the highest voltage level.

OPERATION—TOLERANCE SELECT

The DS1831 provides two TOL inputs for individual customization of the DS1831 to specific application requirements. If the TOL for the 5V supply is tied to the 5V input a 5% tolerance is selected. If the TOL is connected to ground a 10% tolerance is selected or if it is left unconnected a 15% tolerance is selected. If the TOL for the 3.3V supply is tied to the 3.3V input a 5% tolerance is selected, a 10% tolerance is selected if it is connected to ground, and a 20% tolerance is selected if the input is left unconnected. These tolerance conditions are set at power up and can only be changed by power cycling the device.

OPERATION—RESET TIME-DELAY SELECT

The DS1831 provides two TD inputs for individual customization of reset time-delays and an additional one for the DS1831A watchdog. TD inputs select time delays for the $\text{IN}_{5\text{V}}$ and $\text{IN}_{3.3\text{V}}$ resets outputs and the Watchdog on the DS1831A. The reset time delays are shown in Table 1. These allow the selection of minimum delays of 10ms, 100ms, and 1000ms.

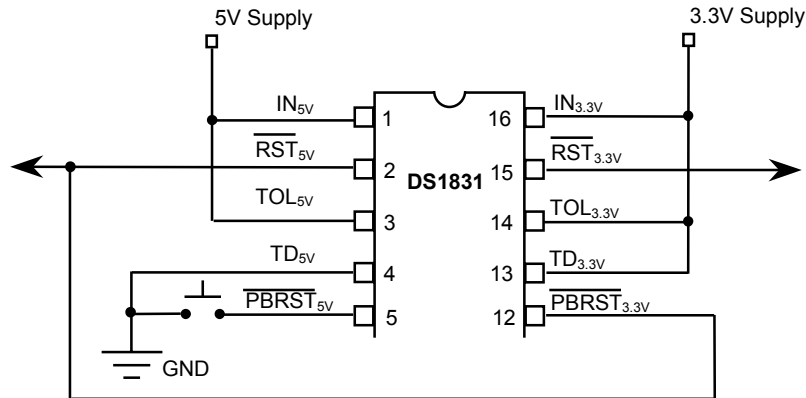
Wiring an individual reset output to the push-button input of the other voltage reset allows custom reset timings or allows for the sequencing of the reset outputs. See Figure 2.

These time-delays are set at power-up and cannot be changed after the device reaches an in-tolerance condition.

TD INPUTS/RESET AND WATCHDOG TIME-DELAYS Table 1

TD	RESET TIME-DELAY		
	MIN	TYP	MAX
GND	10ms	16ms	20ms
Float	100ms	160ms	200ms
V_{CC}	1000ms	1600ms	2000ms

PUSHBUTTON RESET SEQUENCING Figure 2



NOTE: The $\overline{\text{RST}}_{5V}$ output is connected to the $\text{IN}_{3.3V}$ via a 100 k Ω resistor in the push-button input and therefore does not require a pull-up resistor (an addition pull up can be used to accelerate responses). If an external pull up is used in this example it must be connected to the 3.3V power supply.

OPERATION—PUSHBUTTON RESET

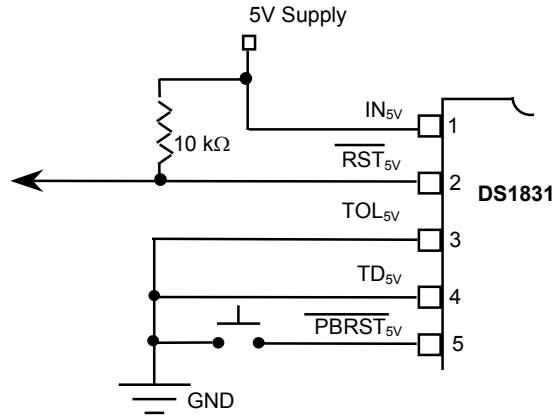
The DS1831 provides three pushbutton inputs for manual reset of the device. Pushbutton inputs for the 3.3V reset, 5V reset, and a master pushbutton reset (DS1831 and DS1831B only) input; provide multiple options for system control. The 3.3V pushbutton reset and 5V pushbutton resets provide a simple manual reset for the associated reset output; while the master pushbutton reset forces all resets and NMI outputs active low.

The 5V reset pushbutton input and the 3.3V reset pushbutton input provide manual reset control input for each associated reset output. When the output associated with a pushbutton input is not active, a pushbutton reset can be generated by pulling the associated $\overline{\text{PBRST}}$ pin low for at least 20 μs . When the pushbutton is held low the reset will be forced active and will remain active for a reset cycle after the pushbutton is released. See Figure 2 for an application example that allows a user to sequence the reset outputs.

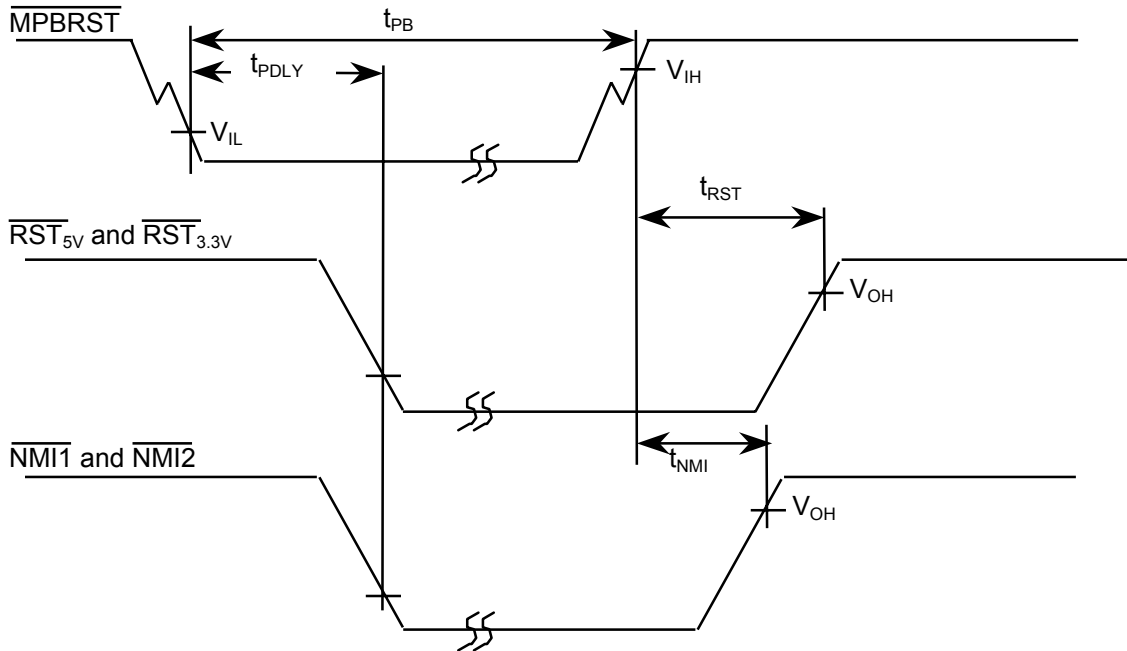
A master pushbutton reset cycle can be started if at least one voltage input (IN_{5V} , $\text{IN}_{3.3V}$, IN_1 , or IN_2) is in tolerance and at least one output is active. A master pushbutton reset is generated by pulling the $\overline{\text{MPBRST}}$ pin low for at least 20 μs . When the pushbutton is held low all outputs are forced active and will remain active for a reset or NMI time delay after the pushbutton is released. The Master Pushbutton input is pulled high through an internal 100k Ω pull up resistor and debounced via internal circuitry. See Figure 3 for an application example. Figures 4 and 5 for the timing diagram.

The 5V and 3.3V pushbutton reset inputs are pulled high through an internal 100k Ω pull up resistor to the voltage input, which is associated with that pushbutton. The master pushbutton is pulled to the greater of the IN_{5V} and $\text{IN}_{3.3V}$ inputs.

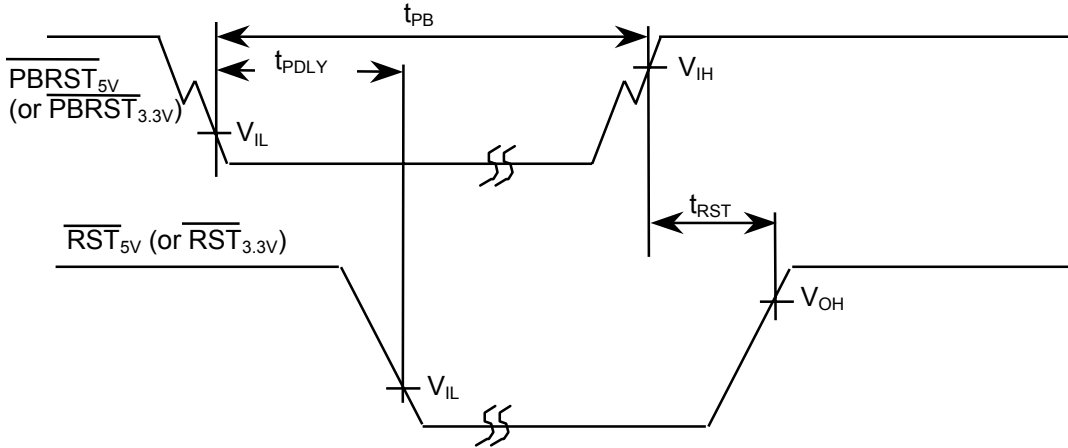
PUSHBUTTON RESET Figure 3



TIMING DIAGRAM—MASTER PUSHBUTTON RESET Figure 4



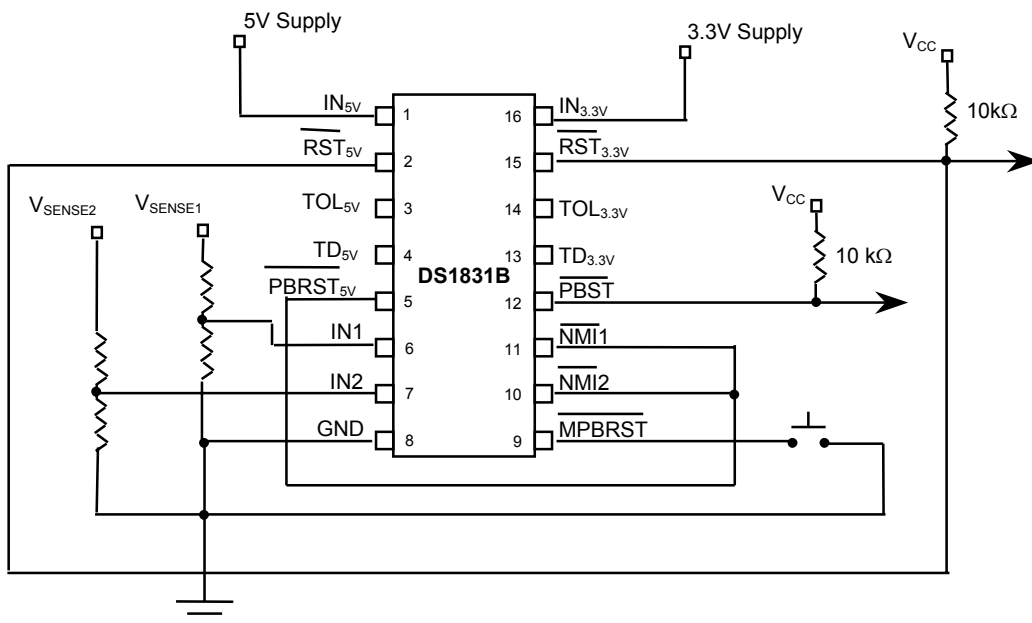
TIMING DIAGRAM—5V OR 3.3V PUSHBUTTON RESET Figure 5



OPERATION—PUSHBUTTON STATUS

The DS1831B provides a master pushbutton status open drain output. The $\overline{\text{PBST}}$ output indicates the status of the most recent reset condition. If the last reset was generated by the master pushbutton input it would maintain a low condition until cleared by another event (except the master pushbutton) generating a reset. Once cleared it will remain high until the master pushbutton is pulled low generating a reset condition. The $\overline{\text{PBST}}$ output is open drain and will require a pull-up resistor on the output to maintain a valid condition. The value of the pull up resistor is not critical in most cases but must be set low enough to pull the output to a high state. A common value used is 10k Ω (see Figure 6).

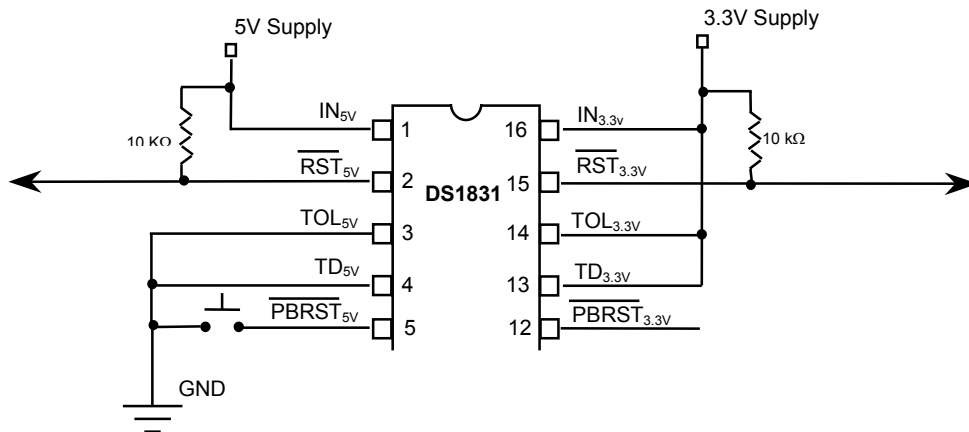
DS1831B APPLICATION EXAMPLE Figure 6



OUTPUT VALID CONDITIONS

The DS1831 can maintain valid outputs as long as one input remains above 1.0V. Accurate voltage monitoring additionally requires that either the 3.3V IN or 5V IN input be above 1.5V. If this condition is not met and at least one of the supply inputs are at or above 1.0V all outputs are maintained in the active condition. The DS1831 requires pull-up resistors on the outputs to maintain a valid output. The value of the pull up resistor is not critical in most cases but must be set low enough to pull the output to a high state. A common pull-up resistor value used is 10k Ω (see Figure 7).

APPLICATION DIAGRAM—OPEN DRAIN OUTPUTS Figure 7



NOTE: If outputs are at different voltages the outputs can not be connected to form a wired AND.

OPERATION—NON-MASKABLE INTERRUPT

The DS1831 has two referenced comparator (DS1831A has only one referenced comparator) that can be used to monitor upstream voltages or other system specific voltages. Each comparator is referenced to the 1.25V internal band gap reference and controls an open-drain output. When a voltage being monitored decays to the voltage sense point, the DS1831 pulses the $\overline{\text{NMI}}$ output to the active state for a minimum 10 μs . The comparator detection circuitry also has built-in hysteresis of 100 μV . The supply must be below the voltage sense point for approximately 2 μs before a low $\overline{\text{NMI}}$ will be generated. In this way, power supply noise is minimized in the monitoring function, reducing false interrupts. See Figure 8 for the non-maskable timing diagram.

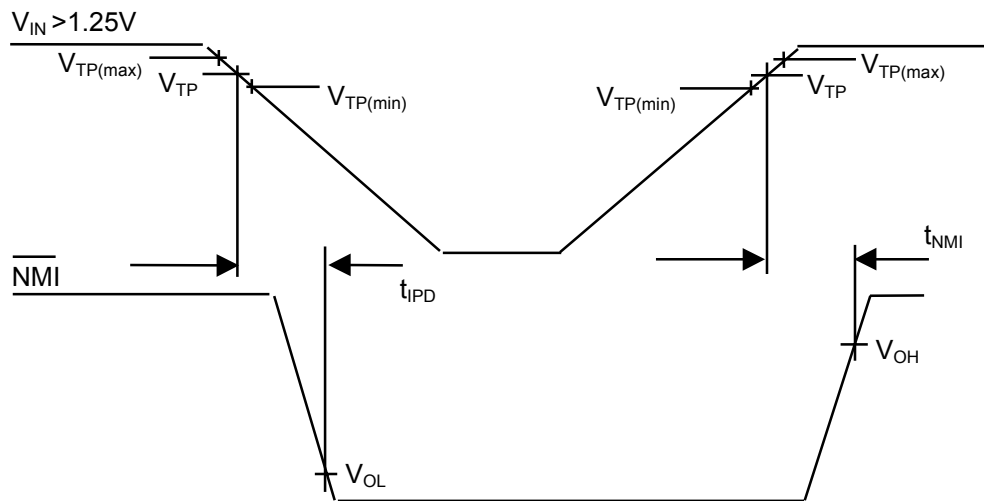
Versatile trip voltages can be configured by the use of an external resistor divider to divide the voltage at a sense point to the 1.25V trip levels of the referenced comparators. See Figure 9 for an example circuit diagram and sample equations. The equations demonstrate a design process to determine the resistor values to use.

Connecting one or both $\overline{\text{NMI}}$ outputs to one of the reset specific $\overline{\text{PBRST}}$ s allows the non-maskable interrupt to generate an automatic reset for the reset time period when an out-of-tolerance condition occurs in a monitored supply. An example is shown in Figure 9.

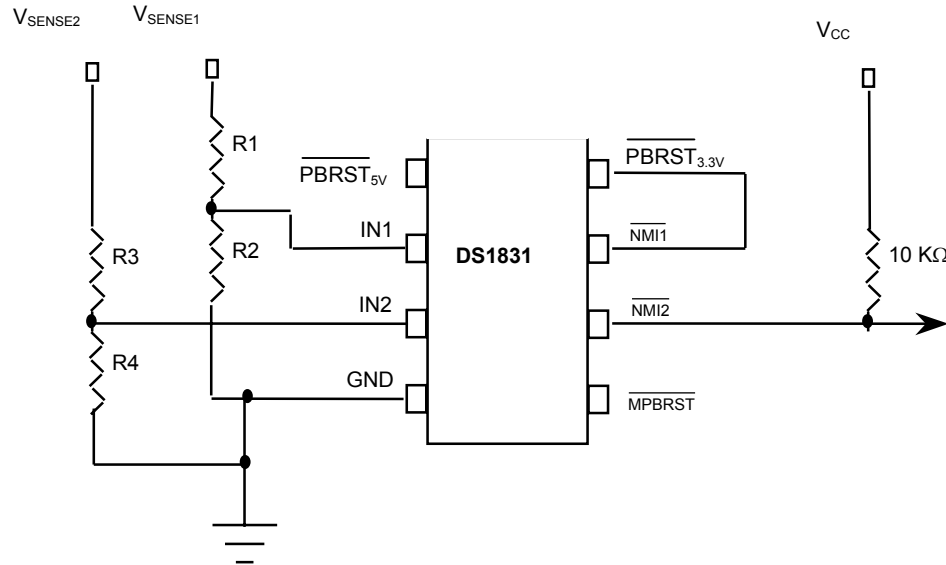
The output associated with the specific input will be held low if the voltage on the input pin is less than 1.25V. If the voltage is above 1.25V the output will not sink current and will be pulled up by the required pull up resistor. The value of the resistors is not critical in most cases but must be set low enough to pull the output to a high state. A common value used is 10k Ω . If a $\overline{\text{NMI}}$ output is connected to a pushbutton input an additional pull-up resistor can be used (to improve speed of transitions) but is not required.

During a power-up, any detected IN pin levels above V_{TP} by the comparator are disabled from generating an inactive (high) interrupt until at least 1 supply on the V_{IN} inputs rises above 1.5 volts. All NMI outputs will be held active (low) until at least one V_{IN} reaches 1.5 volts at which point the $\overline{\text{NMI}}$ outputs will be based on the value of the associated IN input.

TIMING DIAGRAM—NON-MASKABLE INTERRUPT Figure 8



NON-MASKABLE INTERRUPT CIRCUIT EXAMPLE Figure 9



Example: $V_{\text{SENSE1}} = 11.50\text{V}$ trip point $V_{\text{SENSE1}} = \frac{R1 + R2}{R2} \times 1.25\text{V}$

Therefore: $11.50\text{V} = \frac{R1 + 100\text{ k}\Omega}{100\text{ k}\Omega} \times 1.25\text{V}$

Resulting In: $R1 = 820\text{ k}\Omega$

Repeat the same steps to solve for R3 and R4 with V_{SENSE2} .

OPERATION - WATCHDOG TIMER

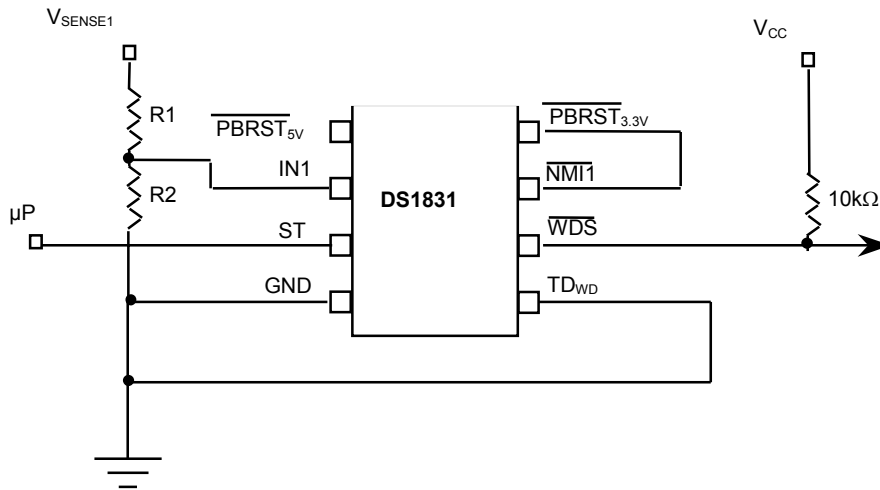
The watchdog timer function (DS1831A only) forces the $\overline{\text{WDS}}$ signal active (low) when the $\overline{\text{ST}}$ input does not have a transition (high-to-low or low-to-high) within the predetermined time period. The time-out period is determined by the condition of the TD_{WD} pin (see Table 1). If TD_{WD} is connected to ground the minimum watchdog time-out would be 10ms, TD_{WD} floating would yield a minimum time-out of 100ms, and TD_{WD} connected to V_{CC} would provide a time-out of 1000ms minimum. Time-out of the watchdog starts when at least one of the $\overline{\text{RST}}$ outputs becomes inactive (high). If a transition occurs on the ST input pin prior to time-out, the watchdog timer is reset and begins to time-out again. If the watchdog timer is allowed to time-out, then the $\overline{\text{WDS}}$ output is pulsed active for a minimum of 100 μs .

The $\overline{\text{WDS}}$ output is an open-drain output and must be pulled up externally. In most applications this output would be connected to one of the Pushbutton inputs and would not require an external pull-up resistor. The value of the resistors is not critical in most cases but must be set low enough to pull the output to a high state. A common value used is 10k Ω . If a $\overline{\text{WDS}}$ output is connected to a pushbutton input an additional pull-up resistor can be used (to improve speed of transitions) but is not required.

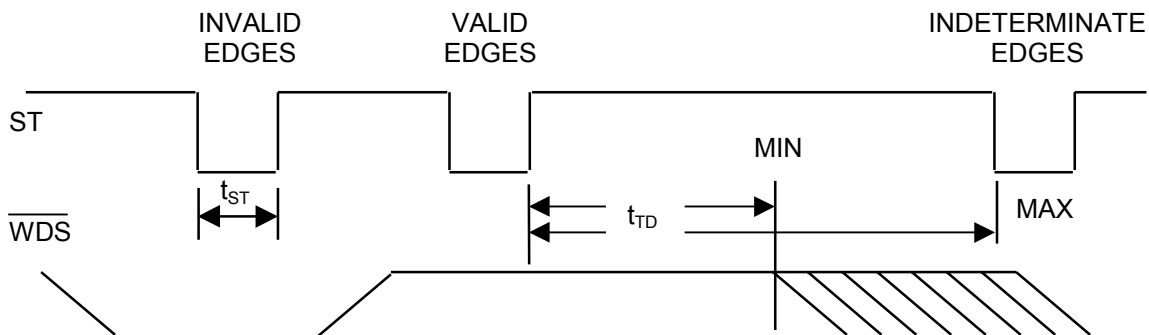
The \overline{ST} input can be derived from many microprocessor outputs. The most typical signals used are the microprocessor address signals, data signals, or control signals. When the microprocessor functions normally, these signals would, as a matter of routine, cause the watchdog to be reset prior to time-out. To guarantee that the watchdog timer does not time-out, a transition must occur at or less than the minimum times shown in Table 1. A typical circuit example is shown in Figure 10. The watchdog timing is shown in Figure 11.

The DS1831A watchdog function cannot be disabled. The watchdog strobe input must be strobed to avoid a watchdog time-out however the watchdog status output can be disconnected yielding the same result.

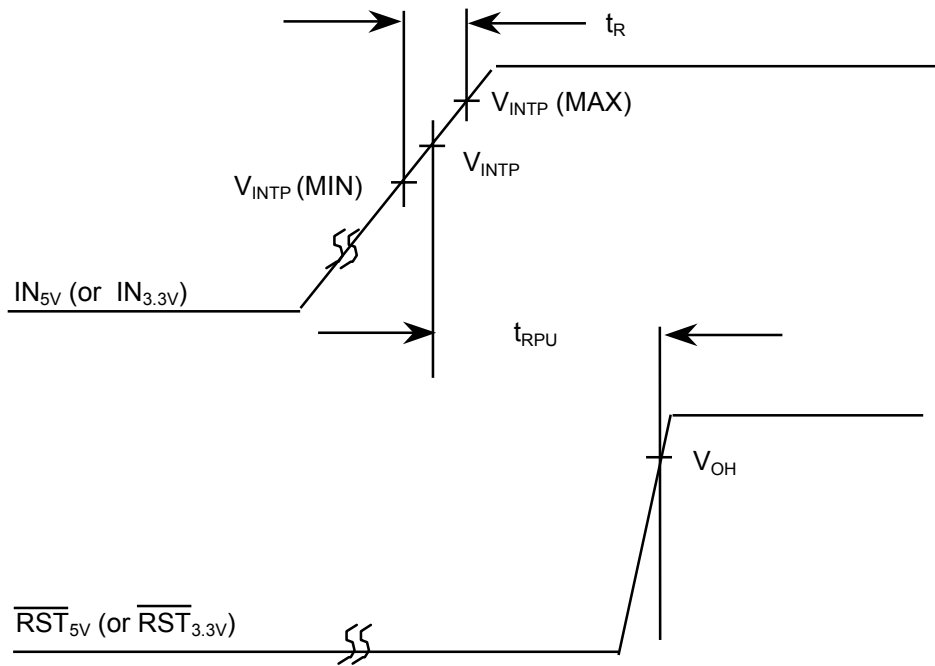
WATCHDOG CIRCUIT EXAMPLE Figure 10



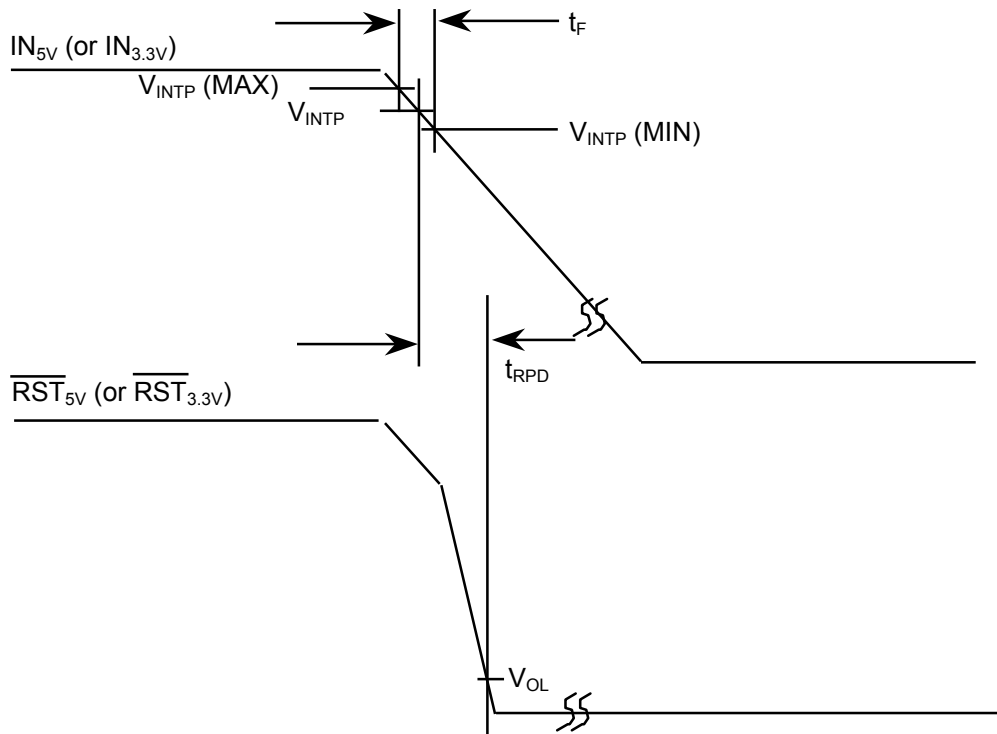
TIMING DIAGRAM — STROBE INPUT Figure 11



RESET TIMING DIAGRAM—POWER UP Figure 12



RESET TIMING DIAGRAM — POWER DOWN Figure 13



ABSOLUTE MAXIMUM RATINGS*

Voltage on IN_{5V} or $IN_{3.3V}$ Pins Relative to Ground	-0.5V to +6.0V
Voltage on either \overline{RST} Relative to Ground	-0.5V to the greater of $IN_{5V} + 0.5V$ or $IN_{3.3V} + 0.5V$
Voltage on $\overline{PBRST}_{3.3V}$ Relative to Ground	-0.5V to $IN_{3.3V} + 0.5V$
Voltage on \overline{PBRST}_{5V} Relative to Ground	-0.5V to $IN_{5V} + 0.5V$
Voltage on \overline{MPBRST} , $IN1$, $IN2$ Relative to Ground	-0.5V to the greater of $IN_{5V} + 0.5V$ or $IN_{3.3V} + 0.5V$
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See IPC/JEDEC J-STD-020A specification

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(-40°C to 85°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
IN_{5V} (Supply Voltage)	V_{IN}	1.0	5.5	V	1
$IN_{3.3V}$ (Supply Voltage)	V_{IN}	1.0	5.5	V	1
$\overline{PBRST}_{3.3V}$, \overline{PBRST}_{5V} , \overline{MPBRST} , ST input High Level	V_{IH}	$0.7 \times V_{INT}$	$V_{INT} + 0.3$	V	1*
$\overline{PBRST}_{3.3V}$, \overline{PBRST}_{5V} , \overline{MPBRST} , ST input Low Level	V_{IL}	-0.3	$0.3 \times V_{INT}$	V	1*

* V_{INT} is the greater voltage level of the IN_{5V} or $IN_{3.3V}$.

DC ELECTRICAL CHARACTERISTICS(-40°C to 85°C; $IN_{3.3V}$, $IN_{5V} = 1.0V$ to $5.5V$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1.0		+1.0	μA	2
Output Current @ 2.4V	I_{OH}					3
Output Current @ 0.4V	I_{OL}	+10			mA	4
Operating Current @ $\leftarrow 5.5V$	I_{CC}		80	100	μA	5
Operating Current @ $\leftarrow 3.6V$	I_{CC}		60	85	μA	6
IN_{5V} Trip Point ($TOL_{5V} = IN_{5V}$)	V_{INTP}	4.50	4.63	4.75	V	
IN_{5V} Trip Point ($TOL_{5V} = GND$)	V_{INTP}	4.25	4.38	4.49	V	
IN_{5V} Trip Point ($TOL_{5V} = Float$)	V_{INTP}	4.00	4.15	4.24	V	
$IN_{3.3V}$ Trip Point ($TOL_{3.3V} = IN_{3.3V}$)	V_{INTP}	2.98	3.06	3.15	V	
$IN_{3.3V}$ Trip Point ($TOL_{3.3V} = GND$)	V_{INTP}	2.80	2.88	2.97	V	
$IN_{3.3V}$ Trip Point ($TOL_{3.3V} = Float$)	V_{INTP}	2.47	2.55	2.64	V	
IN Input Trip Points	V_{TP}	1.15	1.25	1.30	V	

CAPACITANCE $(t_A = +25^\circ\text{C})$

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Input Capacitance	C_{OUT}	7	pF	

AC ELECTRICAL CHARACTERISTICS $(-40^\circ\text{C to } 85^\circ\text{C}; I_{N_{3.3V}}, I_{N_{5V}} = 1.0\text{V to } 5.5\text{V})$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RESET Active Time (T_D =Low)	t_{RST}	10	16	20	ms	5
RESET Active Time (T_D =Float)	t_{RST}	100	160	200	ms	5
RESET Active Time (T_D =High)	t_{RST}	1000	1600	2000	ms	5
V_{CC} Detect to \overline{RST}	t_{RPU}	See RESET Active Time			ms	5
V_{CC} Detect to \overline{RST}	t_{RPD}		2	10	μs	6
V_{IN} Detect to \overline{NMI}	t_{IPD}		2	10	μs	6
NMI Active Time	t_{NMI}	20			μs	
$\overline{PBRST} = V_{IL}$	t_{PB}	20			μs	
\overline{PBRST} Stable Low to Reset Active	t_{PDLY}			50	μs	
Watchdog Timeout ($T_{D(WD)}$ =Low)	t_{TD}	10	16	20	ms	
Watchdog Timeout ($T_{D(WD)}$ =Float)	t_{TD}	100	160	200	ms	
Watchdog Timeout ($T_{D(WD)}$ =High)	t_{TD}	1000	1600	2000	ms	
ST Pulse Width	t_{ST}	10			ns	
V_{in} Slew Rate ($V_{INTP(MAX)}$ to $V_{INTP(MIN)}$)	t_F	300			μs	
V_{in} Slew Rate ($V_{INTP(MAX)}$ to $V_{INTP(MIN)}$)	t_R	0			ns	

NOTES:

- 1) All voltages are referenced to ground.
- 2) All Pushbutton inputs are internally pulled to the associated Supply IN input or the greatest Supply IN input for the \overline{MPBRST} with an internal Impedance of 100k Ω .
- 3) Measured with outputs open and $I_{N_{3.3V}}$ or $I_{N_{5V}} \leq 5.5\text{V}$
- 4) Measured with outputs open and $I_{N_{3.3V}}$ or $I_{N_{5V}} \leq 3.6\text{V}$.
- 5) Measured using $t_R = 5\mu\text{s}$
- 6) Noise immunity - pulses $< 2\mu\text{s}$ at a trip level will not cause a \overline{RST} or \overline{NMI} .

ORDERING INFORMATION

Ordering Part Number	Package Type	Description
DS1831	16-Pin DIP 300mil	5V/3.3V Multisupply Monitor
DS1831S	16-Pin SO 150mil	5V/3.3V Multisupply Monitor
DS1831A	16-Pin DIP 300mil	5V/3.3V Multisupply Monitor w/Watchdog
DS1831AS	16-Pin SO 150mil	5V/3.3V Multisupply Monitor w/Watchdog
DS1831B	16-Pin DIP 300mil	5V/3.3V Multisupply Monitor w/Pushbutton Status
DS1831BS	16-Pin SO 150mil	5V/3.3V Multisupply Monitor w/Pushbutton Status

* Add "/T&R" for tape and reeling of surface mount packages.